## REMARKS

Applicant thanks the Examiner Tung for the courtesy he extended in a telephone interview with Applicant's attorney on July 12, 2005.

These remarks are in reply to the Office Action mailed May 13, 2005. Claims 1-11 stand rejected under 35 U.S.C. 103(a). Claims 1, 6, and 7 have been amended. Claims 12-17, which are directed to graphics display systems, have been added. Applicant respectively traverses the rejections.

Claim Rejections - 35 U.S.C. 103(a)

Claims 1-3 and 6-9 stand rejected under 35 U.S.C. 103(a) as not being patentable over U.S. Pat. to Zhu[1] ("Zhu") in view of U.S. Pat. to Rinaldi, et al.[2] ("Rinaldi").

The Zhu reference "relates to bus controllers for bus transfers between a host device and a slave device."[3] Zhu discloses a data bus 18 and an address bus.[4] The slave device is a memory controller 21.[5] A "slave side bus"[6] couples the slave 21 to a graphics accelerator 15 and a host interface 23.

> "The memory controller 21 is connected through two *alternate data paths* to a host interface 23. One *data path* passes through the graphics accelerator 15, whereas the other *data path* bypasses the graphics accelerator 15."[7]

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[1] No. 5,423,009
[2] No. 6,327,002
[3] Col. 1, lines 12-14
[4] At col. 3, lines 49-50 it is said "Assume further that the address bus (not shown) from the CPU is (n-q) bits wide, represented as A(n . . . q)."
[5] Col. 4, line 3.
[6] Col. 3, lines 42-61.
[7] Col.2 lines 64-68 (emphasis added).

A bus connection between the input of the graphics accelerator 15 and the slave 21, the office action asserts, constitutes a bypassing switching circuit.

A bus connection, however, is not a bypass switching circuit. A bus connection does not couple and decouple an electrical connection. A bus connection does not provide *alternate electrical paths*. By definition, all devices coupled to a bus are permanently coupled to the bus and receive all electrical signals transmitted on the bus. Zhu fails to disclose or suggest either a switching circuit or electrical switching.

The present invention includes a controller select input 23 of the graphics controller 10. The select input 23 is coupled to an enable input E of the video data processor and to a bypass switch 24. When the bypass processing mode is disabled, the bypass switch is *opened*.[8] When the bypass processing mode is disabled, electrical signals sent by the host on the bypass channel never reach a display panel.

As is well known to one skilled in the art, the power required to transmit a signal to two or more devices, such as by placing a signal on a bus, is generally greater than the power required for transmit the same signal to a single device. Thus, the bypass switch of the present invention provides a significant power conservation advantage over the Zhu bus. In battery-powered devices, power conservation is important.

The Zhu reference discloses that the graphics accelerator 15 is connected to a host interface 23 by a slave side bus, and to a memory controller 21. The office action assumes that the host interface and the memory controller, both of which are physically located in the graphics coprocessor, are equivalent to a host and a display device, respectively. This assumption ignores that a graphics controller is provided as a separate

[8] Application, paragraph [0018]

chip between a host and a display device.[9] This assumption also ignores that the input bus of a preferred graphics controller is coupled directly to the output bus of the host, and the output bus of the graphics controller is coupled directly to the graphics display device. Preferred embodiments of the present invention permit the host to communicate *directly* with the graphics display device.[10] Further, this assumption ignores the advantages provided in permitting such direct communication. Preferred embodiments permit avoiding:

> "storing and processing data in the graphics controller chip where that is desired, including avoiding the necessity to synchronize the movement of data through the graphics controller chip."[11]

Thus, the present invention permits avoiding what cannot be avoided in the Zhu device, at least not without changing the fundamental operating characteristics of the device . For example, the Zhu host interface 23 "generates the exact number of slave cycles required to generate a host request."[12] As another example, the Zhu host interface 23 is connected to a bus interface 25, which "includes a FIFO and address comparison circuitry."[13] Similar examples may be provided with respect to Zhu memory controller 21.

In order find a teaching for coupling an input bus of a graphics controller directly to the output bus of a host (or for coupling an output bus of a graphics controller to the input bus of a display), it would be necessary to modify Zhu so that the Zhu device neither stores data that "bypasses" the graphics accelerator or controls the transmission

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[9] Application, paragraph [0002]
[10] Application, paragraph [0018]
[11] Application, paragraph [0019]
[12] No. 5,423,009, Col. 3, lines 34-35.
[13] No. 5,423,009, Col. 3, lines 2-3.

cycles of such data. However, such modifications would change the principle of operation of the Zhu device and render it unsatisfactory for its intended purpose. Accordingly, the teachings of Zhu are insufficient to render the claims of the present invention prima facie obvious.

The claims have been amended to clarify that the bypass switching circuit is adapted to electrically couple and decouple the input bus of the graphics controller to the output bus. Further, the claims have been amended to clarify that in some embodiments the graphics controller includes a select input for receiving a signal for opening and closing the bypass switch. In addition, new claims 12-17 emphasize that the input bus of the graphics controller is directly coupled to the output bus of the host, and the output bus of the graphics controller is coupled directly to the graphics display device.

Claims 4-5 and 10-11 stand rejected under 35 U.S.C. 103(a) as not being patentable over U.S. Pat. to Zhu[14] ("Zhu") in view of U.S. Pat. to Rinaldi, et al.[15] ("Rinaldi"), and further in view of U.S. Pat. to Fuimoto[16] and U.S. Pat. to Clark[17].

Claims 4-5 and 10-11, however, depend from independent claims 1 and 6 are patentable for the same reasons expressed above that claims 1 and 6 are patentable.

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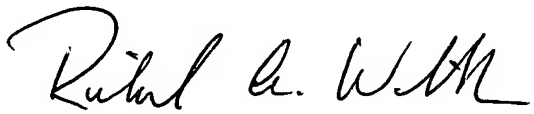
[14] No. 5,423,009
[15] No. 6,327,002
[16] No. 5,479,183
[17] No. 5,949,437

Conclusion

Accordingly, claims 1-17 are in condition for allowance. Applicant respectively requests that claims 1-17 be allowed, and this application be passed to issue.

Respectfully submitted,



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